

High Speed Multi-lane LVDS Inter-FPGA Communication Link

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Abstract

Systems employing multiple FPGAs to handle distributed processing require data communication among FPGAs for unified operation. This paper describes implementation of a multi-lane Low Voltage Differential Signaling (LVDS) interface to form 10 Gbps full duplex communication link interconnecting multiple FPGAs on a board. The design utilizes advanced IO resources available in the latest Virtex and Spartan series of FPGAs from Xilinx. We also developed a Bit Error Rate Tester for evaluating each individual LVDS physical lane operating at 625 Mbps. Challenges involved in the board design, related to implementation of the interface, are also discussed in this paper.