

Implementing FPGA based PCI Express design

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Abstract

PCI Express (Peripheral Component Interconnect Express) abbreviated as PCIe or PCI-E, is designed to replace the older PCI, PCI-X, and AGP standards. PCIe 2.1 or Gen2 is the latest standard for expansion cards that has come out recently on mainstream personal computers. Conceptually, the PCIe bus can be thought of as a high-speed serial replacement of the older parallel PCI/PCI-X bus. At the software level, PCIe preserves compatibility with PCI; a PCIe device can be configured and used in legacy applications and operating systems that have no direct knowledge of PCIe's newer features. Different solutions for the implementation of PCIe design using FPGAs are available through couple of vendors including Xilinx and Altera. The designer can implement PCIe inside an FPGA by either developing the complete PCIe protocol or by purchasing a readily available IP from the market. Xilinx has both a Soft IP as well as a Hard IP available to the designer to get started with the design. In this paper we present our PCIe implementation in various Xilinx family of devices and further show the advantages and disadvantages with each.